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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,492	09/30/2003	Georg Braun	MUH-12827	6045

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EXAMINER	
PATEL, PARESH H	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,492	BRAUN ET AL.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8 and 9* is/are allowed.

6)☒ Claim(s) *1-7 and 10-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a) because they fail to show DDR interface as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Element 42 as shown in fig. 3 is not found in specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 7, what is not near is "a reaction to an operation condition". For example: what type of reaction? Specification does not support this and hence it is indefinite.

Claim Objections

Claim 1 is objected to because of the following informalities: at line 12 "device" should read --devices--. Appropriate correction is required.

Claim 7 is objected to because of the following informalities: a reaction to an operating condition is not clear from the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art fig. 1-2 and in view of Wyers et al. (US 2004/0201416 A1).

Regarding claim 1, Applicant admitted prior art fig. 1-2 (hereafter APA) discloses a method for calibrating interface devices, which comprises the steps of:

a) providing a plurality of semiconductor devices [see 1' in fig. 2] each having the interface devices [6], a calibration unit [3] connected to the interface devices, a calibration connection [32], and a calibration path [31] connected to the calibration connection;

c) calibrating the interface devices in the first semiconductor device [using 2, 3 and 5];

APA discloses all the elements except for **a switching unit** disposed in the calibration path for controlling and switching the calibration path; b) generating, in a first semiconductor device of the semiconductor device, an active calibration signal connecting the calibration unit to the calibration connection using the switching unit; d) generating a passive calibration signal isolating the calibration unit from the calibration

connection using the switching unit; and e) repeating steps b), c) and d) for all further semiconductor devices of the semiconductor devices.

However, APA calibrates the interface device [6] using calibration reference [5]. Wyers et al. (hereafter Wyers) in fig. 22 discloses **a switching unit** [1504 or 1508 or 1514 or 1516] which is controlled by a processor [1210, see fig. 12], which also has calibration reference [i.e. calibration value]. Wyers also deal with calibration method [see, Title] for driver interface. Wyers also discloses generating, in a first semiconductor device of the semiconductor devices, an active calibration signal [using 1210] connecting the calibration unit [calibration engine 118] to the calibration connection [1506] using the switching unit [1504]; d) generating [using 118] a passive calibration signal [when 1504 is open] isolating the calibration unit from the calibration connection using the switching unit.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use **a switching unit , active and passive calibration signal** as taught by Wyers, in order to obtain control over signals passing through switching unit during calibration.

APA discloses plurality of semiconductor devices. Wyer is silent about calibrating plurality of semiconductor devices. APA discloses calibrating plurality of plurality of semiconductor devices individually using data lines DQ and calibration reference 5. Repeating the same steps for a plurality of semiconductor device is art-recognize equivalent at the time the invention was made. Therefore, repeating steps b), c) and d) for a plurality of semiconductor devices is obvious over the combination APA and

Wyers, since combination of APA and Wyers discloses calibrating semiconductor device using steps b), c) and d) as mentioned above.

Regarding claim 2, The combination of APA and Wyers as mentioned above discloses the calibration method according to claim 1, wherein the repeating step comprises repeating cyclically the steps b) through e).

Regarding claim 5, APA discloses the calibration method according to claim 1, which further comprises forming the semiconductor devices as memory chips having a double data rate interface [6].

Regarding claim 6, APA discloses the calibration method according to claim 1, which further comprises using the interface devices as output drivers [6] for outputting data signals on data signal lines and/or terminations for low-reflection termination of the data signal lines [due to calibration of 6].

Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA and Wyers as applied to claim 1 above, and further in view of Yada (US 4559521).

Regarding claim 3, the combination of APA and Wyers discloses all the elements including providing each of the semiconductor devices with an instruction evaluation unit [2 of APA, see fig. 1] being connected to control and address connections [21 of APA, see fig. 1] on a respective semiconductor device [1' of APA, see fig. 1], the control and address connections being provided for connecting to a control and address bus [CA of APA, see fig. 1]. APA and Wyers is silent about generating the active calibration signal in the instruction evaluation unit on a basis of a calibration instruction transmitted via the

control and address bus. However, Yada in fig. 2 and lines 31-48 of column 3 discloses generating the active calibration signal in the instruction evaluation unit [24 and 25] on a basis of a calibration instruction [from 25] transmitted via the control and address bus [26].Yada discloses calibration of A-D converter. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use instruction evaluation unit on a basis of a calibration instruction as taught by Yada to modify the instruction unit of APA to achieve the calibration of higher order integration periods.

Regarding claim 4, Yada discloses the calibration method according to claim 3, which further comprises: connecting the instruction evaluation unit [24] to at least one respective data connection for connecting to a data line [data line for 27]; and generating [using 24] the active calibration signal on a basis of a data signal transmitted via the data line [lines 56-61 of column 3, also see fig. 8].

Claims 10-14 is rejected under 35 U.S.C. 103(a) as being unpatentable over APA and in view of Yada.

Regarding claims 10 and 14, APA in fig. 1-2 discloses a semiconductor device (plurality for claim 14), comprising:

control and address connections [21] for connecting to a control and address bus;

data connections [22] for connecting to a data bus;

a calibration connection [32] for connecting to a calibration reference;

an instruction evaluation unit [2] connected to said control and address connections;

a calibration path [31];

a calibration unit [3] connected to said calibration connection through said calibration path.

APA discloses all the elements except for **a calibration signal path**; and **a switching unit** integrated in said calibration path for opening and closing said calibration path, said switching unit coupled to said instruction evaluation unit through said calibration signal path, said instruction evaluation unit controlling said switching unit on a basis of calibration instructions transmitted via the control and address bus.

Yada in fig. 2 discloses calibrating A-D converter using a calibration path [path from 37 to 21 and 22 respectively] and switching unit [21, 22] for opening and closing said calibration path, said switching unit coupled to said instruction evaluation unit [24] through said calibration signal path, said instruction evaluation unit controlling said switching unit on a basis of calibration instructions [from 25] transmitted via the control and address bus [26]. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify APA to add switching unit and calibration path as taught by Yada, to achieve calibration for higher order integration periods.

Regarding claim 11, Yada discloses the semiconductor device according to claim 10, wherein said switching unit is controlled on a basis of a data signal transmitted via at least one data line [26, 31].

Regarding claim 12, APA discloses the semiconductor device according to claim 10, wherein the semiconductor device is a memory chip [1'] and has a double data rate interface [6].

Regarding claim 13, APA in fig. 1 discloses the semiconductor device according to claim 10, further comprising output drivers [6] which can be calibrated using the calibration reference [5] for outputting data signals on data signal lines.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter: No prior art has been found that meets all the limitation of claim 8 calling for a method for operating a plurality of semiconductor devices each connected to a common calibration reference and disposed to form a data bus system having a control and address bus and an at least partially common data bus, which comprises the steps of: connecting a calibration connection to a calibration unit in a respectively addressed semiconductor device; and switching the calibration connection to a high impedance state after completing a calibration process, as further defined at claim 8.

Claim 9 is allowed because it depends from allowable claim 8.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 572-272-1968. The examiner can normally be reached on 8:00 to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paresh Patel
February 13, 2005